

FIGURE 3

003261.7008X

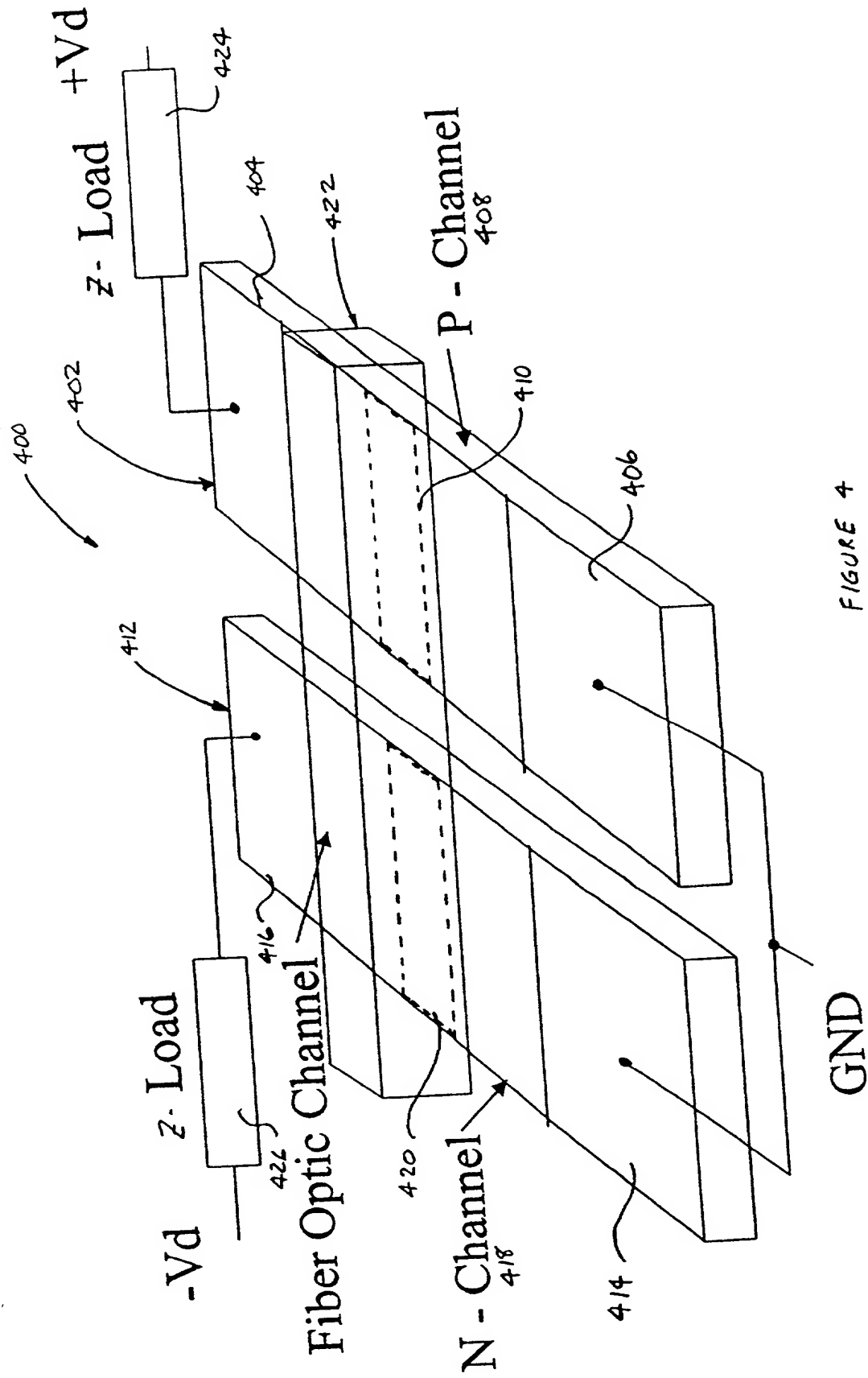


FIGURE 4  
PAGE 3 OF 5

FIG. 5 is a schematic diagram of a semiconductor device 500 in accordance with one embodiment of the present invention. The device 500 includes a substrate 502, a gate stack 504, a source region 506, a drain region 508, and a channel region 510. The gate stack 504 is formed over the substrate 502 and includes a gate dielectric layer 512 and a gate electrode layer 514. The source region 506 and drain region 508 are formed in the substrate 502 on opposite sides of the channel region 510. The channel region 510 is formed in the substrate 502 beneath the gate stack 504. The device 500 is configured to operate as a transistor. The gate electrode layer 514 is connected to a gate voltage V<sub>g</sub>. The source region 506 is connected to a source voltage V<sub>s</sub>. The drain region 508 is connected to a drain voltage V<sub>d</sub>. The channel region 510 is connected to a load resistor 516. The load resistor 516 is connected to a load voltage V<sub>L</sub>. The device 500 is configured to operate as a transistor. The gate electrode layer 514 is connected to a gate voltage V<sub>g</sub>. The source region 506 is connected to a source voltage V<sub>s</sub>. The drain region 508 is connected to a drain voltage V<sub>d</sub>. The channel region 510 is connected to a load resistor 516. The load resistor 516 is connected to a load voltage V<sub>L</sub>.

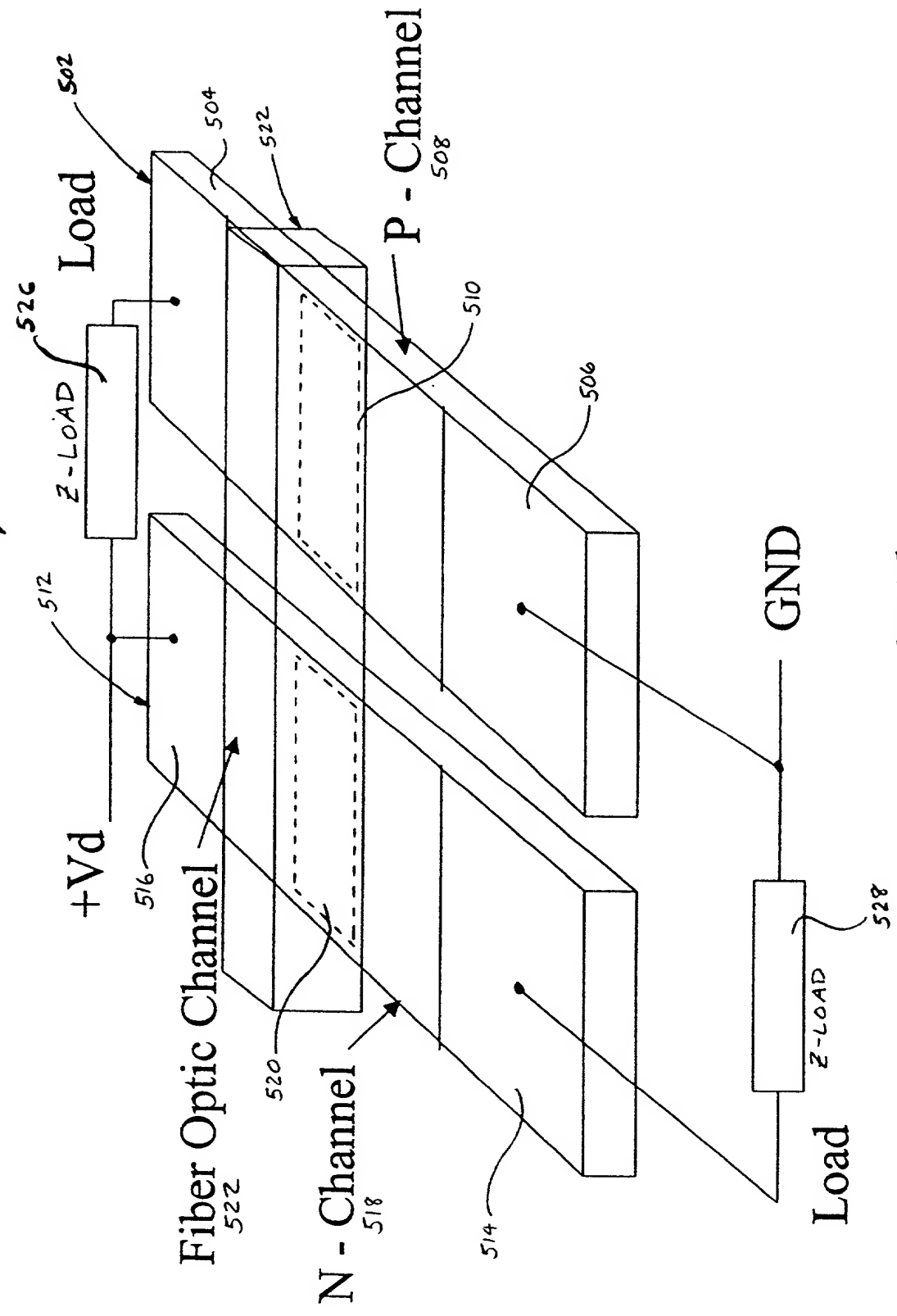


FIGURE 5  
PAGE 4 OF 5

FIG. 6 is a schematic diagram of a device 600 in accordance with the present invention.

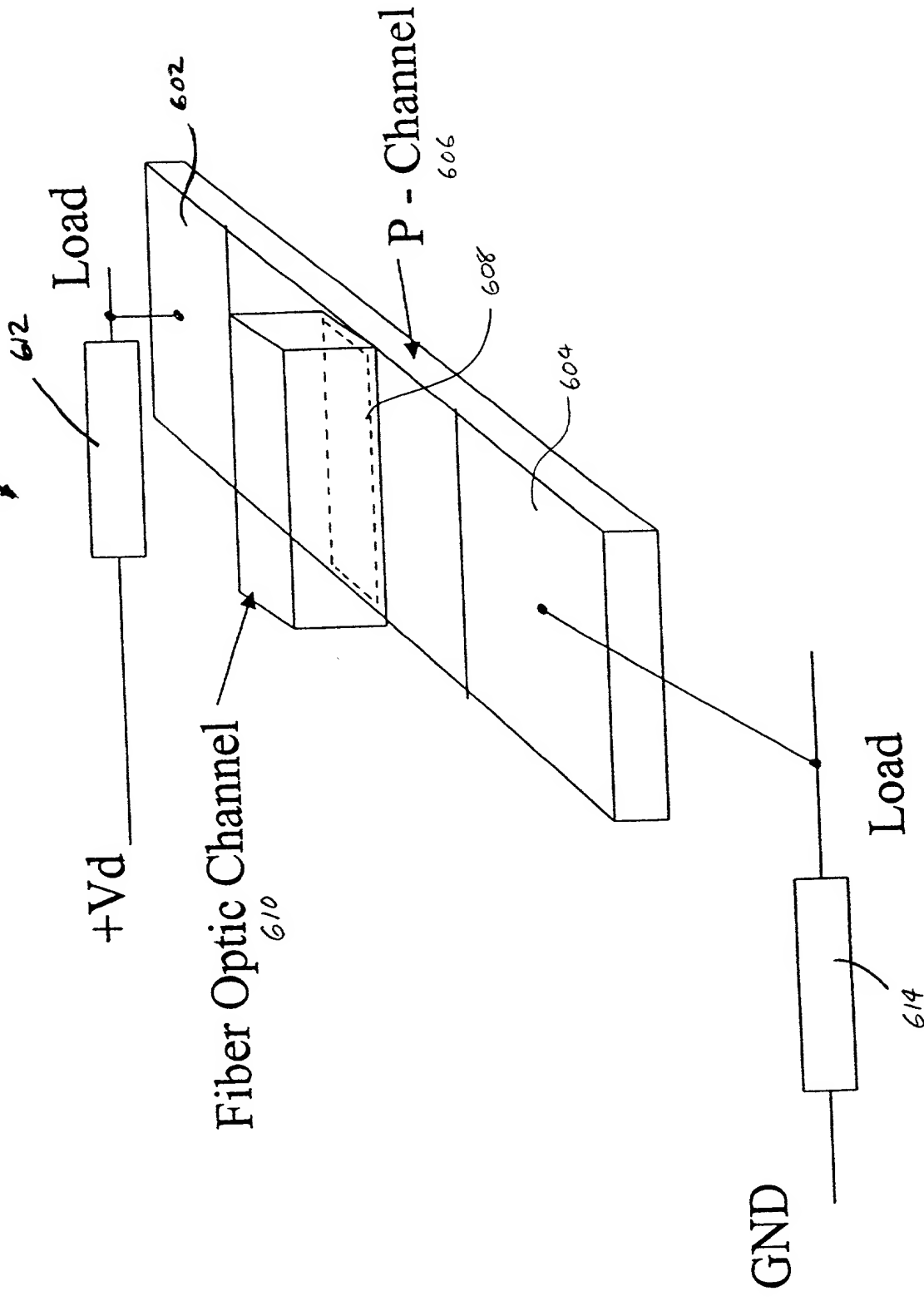


FIGURE 6